AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of accessing data storage locations in a memory circuit comprising the acts of:

issuing at least one memory access control signal to a first portion of ~~said~~ the memory circuit;

determining, in a state machine, based upon the memory access control signal, whether to couple a data bus to a second portion of the memory circuit, wherein the state machine comprises a programmable gate array; and

coupling a data bus to a the second portion of ~~said~~ the memory circuit in response to a determination of the state machine ~~said at least one memory access control signal~~.

2. (Original) The method of Claim 1, wherein issuing at least one memory access control signal comprises issuing a row address strobe signal and a column address strobe signal.

3. (Original) The method of Claim 1, wherein issuing at least one memory access control signal comprises issuing a memory circuit enable signal.

4. (Original) The method of Claim 1, wherein coupling a data bus comprises closing a transfer gate in each line of said data bus.

5. (Currently Amended) A method of accessing data storage locations in a memory circuit comprising the acts of:

issuing at least one memory access control signal to a first portion of said memory circuit, the signal comprising a row address strobe signal and a column address strobe signal;

determining, in a state machine, based upon the memory access control signal, whether to couple a data bus to a second portion of the memory circuit, wherein the state machine comprises a programmable gate array; and

coupling a data bus to a second portion of said memory circuit in response to a determination of the state machine ~~said at least one memory access control signal~~, the coupling comprising closing a transfer gate in each line of ~~said~~ the data bus.

6. (Currently Amended) A system for accessing data storage locations in a memory circuit comprising the acts of:

means for issuing at least one memory access control signal to a first portion of said memory circuit; ~~and~~

a state machine configured to determine based upon the memory access control signal, whether to couple a data bus to a second portion of the memory circuit, wherein the state machine comprises a programmable gate array; and

means for coupling a the data bus to a the second portion of said memory circuit in response to a determination of the state machine ~~to said at least one memory access control signal~~.

7. (Original) The system of Claim 6, wherein the means for issuing at least one memory access control signal comprises means for issuing a row address strobe signal and a column address strobe signal.

8. (Original) The system of Claim 6, wherein the means for issuing at least one memory access control signal comprises means for issuing a memory circuit enable signal.

9. (Original) The system of Claim 6, wherein the means for coupling a data bus comprises means for closing a transfer gate in each line of said data bus.

10. (Currently Amended) A system for accessing data storage locations in a memory circuit comprising the acts of:

means for issuing at least one memory access control signal to a first portion of said memory circuit, the signal comprising a row address strobe signal and a column address strobe signal;

a state machine configured to determine based upon the memory access control signal, whether to couple a data bus to a second portion of the memory circuit, wherein the state machine comprises a programmable gate array; and

means for coupling a the data bus to a the second portion of said memory circuit in response to a determination of the state machine ~~said at least one memory access control signal~~, the coupling comprising closing a transfer gate in each line of ~~said~~ the data bus.

11. (Currently Amended) A device for accessing data storage locations in a memory circuit comprising the acts of:

a component for issuing at least one memory access control signal to a first portion of said memory circuit;

a state machine configured to determine based upon the memory access control signal, whether to couple a data bus to a second portion of the memory circuit, wherein the state machine comprises a programmable gate array; and

a component for coupling a data bus to a second portion of ~~said~~ the memory circuit in response to a determination of the state machine, wherein the state machine comprises a programmable gate array ~~said at least one memory access control signal~~.

12. (Original) The device of Claim 11, additionally comprising a component for issuing a row address strobe signal and a column address strobe signal.

13. (Original) The device of Claim 11, additionally comprising a component for issuing at least one memory access control signal comprises issuing a memory circuit enable signal.

14. (Currently Amended) The device of Claim 1, additionally comprising a component for coupling a data bus comprises closing a transfer gate in each line of ~~said~~ the data bus.

15. (Currently Amended) A device for accessing data storage locations in a memory circuit comprising, the device comprising :

a component for issuing at least one memory access control signal to a first portion of said memory circuit, the signal comprising a row address strobe signal and a column address strobe signal; and

a component for coupling a data bus to a second portion of said memory circuit in response to said at least one memory access control signal, the coupling comprising closing a transfer gate in each line of ~~said~~ the data bus, wherein the component for coupling a data base comprises a state machine for determining when to couple the data bus to the second portion of the memory circuit, wherein the state machine comprises a programmable gate array.